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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/059,691	01/29/2002	Larry D. Hewitt	5500-73200	5930

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EXAMINER	
PHAN, RAYMOND NGAN	

ART UNIT	PAPER NUMBER
2111	4

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/059,691	Applicant(s) HEWITT ET AL.	
	Examiner Raymond Phan	Art Unit 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-47 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-47 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Part III DETAILED ACTION

Notice to Applicant(s)

1. This application has been examined. Claims 1-47 are pending.

2. The Group and/or Art Unit location of your application in the PTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Group Art Unit 2111.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-47 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Avery (US No. 6,691,185) in view of Keller et al. (US No. 6,557,048).

In regard to claims 1, 18, 20-21, Avery discloses a computer system comprising a processor; a plurality of input/output (I/O) nodes serially coupled to the processor through a plurality of packet bus links (see abstract), wherein each of the plurality of I/O nodes includes an upstream packet bus interface, a downstream packet bus interface (see figure 3, col. 3, line 51 through col. 4, line 29). But

Avery does not specifically disclose the peripheral interface bus, the I/O tunnel; a peripheral bus coupled to the peripheral bus interface of one of the plurality of I/O nodes; wherein the one of the plurality of I/O nodes is configured, in the first mode, to selectively convey particular packets through the I/O tunnel between the upstream packet bus interface and the downstream packet bus interface and to the selectively convey packets from the upstream packet bus interface to the peripheral bus interface, and in the second mode, to replicate electrical signals corresponding to packets passing through the I/O tunnel on the peripheral bus. However Keller et al. disclose the processing node 16 comprising a I/O tunnel 34, memory controller 22C connected to the memory 20C (see figure 2); wherein the one of the plurality of I/O nodes is configured, in the first mode, to selectively convey particular packets through the I/O tunnel between the upstream packet bus interface and the downstream packet bus interface and to the selectively convey packets from the upstream packet bus interface to the peripheral bus interface, and in the second mode, to replicate electrical signals corresponding to packets passing through the I/O tunnel on the peripheral bus (see col. 13, line 61 through col. 15, line 33). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Keller et al. within the system of Avery because it would provide the properly ordered transactions within I/O nodes and preserve memory coherency.

In regard to claims 2, 19, 27, 29, Keller et al. disclose wherein in the first mode, the computer system is configured to generate cycles on the peripheral bus in response to the particular packets being selectively conveyed from the upstream packet bus interface to the peripheral bus interface (see col. 8, lines 10-45). Therefore, it would have been obvious to a person of an ordinary skill in the art at

the time the invention was made to have combined the teachings of Keller et al. within the system of Avery because it would provide the properly ordered transactions within I/O nodes and preserve memory coherency.

In regard to claims 3, 30, Keller et al. disclose wherein the peripheral bus includes a peripheral bus connector (see col. 7, lines 7-63). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Keller et al. within the system of Avery because it would provide the properly ordered transactions within I/O nodes and preserve memory coherency.

In regard to claims 4, 31-32, even though the teachings of Keller et al. or Avery do not disclose a dummy card for the signal analyzer connected thereto, however one skilled in the art would have understood that they can choose to have an add-in card to expand the functionality of the computer system.

In regard to claims 5, 33, even though the teachings of Keller et al. or Avery do not disclose wherein the signal analyzer is a logic analyzer, however one skilled in the art would have understood that they can choose to have a logic analyzer to diagnostic the system.

In regard to claims 6, 34-35, even though the teachings of Keller et al. or Avery do not disclose wherein the signal analyzer is a logic analyzer and wherein the signal analyzer is configured to be inserted into the peripheral bus connector, however one skilled in the art would have understood that they can choose to have a signal analyzer is a logic analyzer and wherein the signal analyzer is configured to be inserted into the peripheral bus connector to diagnostic the computer system.

In regard to claims 7, 37, Avery discloses wherein the computer system is configured for performing upstream packet transactions and downstream packet

transactions, wherein the downstream packet transactions originate at the processor and wherein the upstream packet transactions terminate at the processor (see figure 3, col. 3, line 51 through col. 4, line 29).

In regard to claims 8, 22, 38, Keller et al. disclose wherein the I/O node is further configured to, in the second mode, to provide an indication of whether a given packet for which electrical signals are replicated is being conveyed upstream or downstream (see col. 13, line 61 through col. 15, line 33). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Keller et al. within the system of Avery because it would provide the properly ordered transactions within I/O nodes and preserve memory coherency.

In regard to claims 9, 23, 43, Keller et al. disclose wherein in the I/O node includes an arbitration unit, wherein the in second mode, the arbitration unit is configured to determine the order in which electrical signals from a first packet will be replicated relative to electrical signals from the second packet (see col. 13, line 61 through col. 15, line 33). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Keller et al. within the system of Avery because it would provide the properly ordered transactions within I/O nodes and preserve memory coherency.

In regard to claims 10, 24, 39, Keller et al. disclose wherein the I/O node include a command register, wherein the command register is configured to store one or more bits indicative of whether the I/O node is operating in the first mode or the second mode (see col. 13, lines 41-60). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to

have combined the teachings of Keller et al. within the system of Avery because it would provide the properly ordered transactions within I/O nodes and preserve memory coherency.

In regard to claims 11, 25, 40, Keller et al. disclose wherein the I/O node is configured to enter the second mode responsive to inputting one or more signals corresponding to the one or more bits into the command register (see col. 15, line 37 through col. 16, line 38). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Keller et al. within the system of Avery because it would provide the properly ordered transactions within I/O nodes and preserve memory coherency.

In regard to claims 12, 41, even though the teachings of Keller et al. or Avery do not specifically disclose wherein the inputting is perform during a power-on test, however one skilled in the art would have understood that they can choose to implement the reset during the power-on test to fulfill their design and functionality

In regard to claims 13, 44, Avery discloses wherein the peripheral bus is a PCI bus (see col. 1, lines 20-27).

In regard to claims 14, 45, Avery discloses wherein the peripheral bus is a AGP bus (see col. 1, lines 2-27).

In regard to claims 15, 46, even though the teachings of Keller et al. or Avery do not disclose wherein the peripheral bus is a general-purpose instrument bus (GPIB) bus, however one skilled in the art would have understood that they can choose to have general-purpose bus to fulfill their design and functionality.

In regard to claims 16, 42, Keller et al. disclose wherein the electrical signals are replicated onto one or more signals lines on the peripheral bus (see col. 13, line

61 through col. 15, line 33). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Keller et al. within the system of Avery because it would provide the properly ordered transactions within I/O nodes and preserve memory coherency.

In regard to claims 17, 47, Keller et al. disclose wherein the peripheral bus interface is configured in the first mode to convey packets into the I/O tunnel (see col. 13, line 61 through col. 15, line 33). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Keller et al. within the system of Avery because it would provide the properly ordered transactions within I/O nodes and preserve memory coherency.

In regard to claims 28, 36, Avery discloses a computer system comprising a processor; a plurality of input/output (I/O) nodes serially coupled to the processor through a plurality of packet bus links (see abstract), wherein each of the plurality of I/O nodes includes an upstream packet bus interface, a downstream packet bus interface (see figure 3, col. 3, line 51 through col. 4, line 29). But Avery does not specifically disclose the peripheral interface bus, the I/O tunnel; a peripheral bus coupled to the peripheral bus interface of one of the plurality of I/O nodes; wherein the one of the plurality of I/O nodes is configured, in the first mode, to selectively convey particular packets through the I/O tunnel between the upstream packet bus interface and the downstream packet bus interface and to the selectively convey packets from the upstream packet bus interface to the peripheral bus interface, and in the second mode, to replicate electrical signals corresponding to packets passing through the I/O tunnel on the peripheral bus. However Keller et al. disclose the processing node 16 comprising a I/O tunnel 34, memory controller 22C connected

to the memory 20C (see figure 2); wherein the one of the plurality of I/O nodes is configured, in the first mode, to selectively convey particular packets through the I/O tunnel between the upstream packet bus interface and the downstream packet bus interface and to the selectively convey packets from the upstream packet bus interface to the peripheral bus interface, and in the second mode, to replicate electrical signals corresponding to packets passing through the I/O tunnel on the peripheral bus (see col. 13, line 61 through col. 15, line 33). Even though the teachings of Keller et al. or Avery do not disclose wherein the signal analyzer is a logic analyzer and wherein the signal analyzer is configured to be inserted into the peripheral bus connector, however one skilled in the art would have understood that they can choose to have a signal analyzer is a logic analyzer and wherein the signal analyzer is configured to be inserted into the peripheral bus connector to diagnostic the computer system. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Keller et al. within the system of Avery because it would provide the properly ordered transactions within I/O nodes and preserve memory coherency.

Conclusion

6. All claims are rejected.

7. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Kessler et al. (US No. 5,864,738) disclose a massively parallel processing system using two data paths: one connecting to the router circuit to the

interconnect network and the other connecting router circuit to the I/O controller.

Nguyen et al. (US No. 6,539,439) disclose a method and apparatus for interfacing a bus at an independent rate within input/output devices.

Miller et al. (US No. 6,247,058) disclose a method and apparatus for processing network packets using time stamps.

Lai et al. (US No. 6,546,448) disclose a method and apparatus for arbitrating access to a PCI bus by a plurality of functions in multi-function master.

Gibart et al. (US No. 6,484,215) disclose a system having I/O module number assignment utilizing module number signal line having pair of intputs adapted for receiving module number signal and propagation of module number signal down stream.

Chao (US No. 6,115,551) discloses a system for minimizing the number of control signals and maximizing channel utilization between an I/O bridge and a data buffer.

Clouser et al. (US No. 5,884,053) disclose a connector for higher performance PCI with differential signaling.

Sugawara et al. (US No. 6,728,822) disclose a bus bridge circuit, information processing system and cardbus controller.

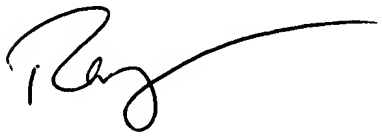
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (703) 306-2756. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (703) 305-9656 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (703) 872-9306.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to **[raymond.phan@uspto.gov]**.

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.



Raymond Phan
5/1/04